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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,613	11/26/2003	Joanna Aizenberg	100.2496	7089

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PRIEST & GOLDSTEIN PLLC
5015 SOUTHPARK DRIVE
SUITE 230
DURHAM, NC 27713-7736

EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,613	AIZENBERG ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-20* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1, 2, and 5-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Dimitrakopoulos et al.. As to claim 1, Dimitrakopoulos et al., Figure 4, discloses a semiconductor apparatus, comprising: a substrate (10) having a substrate surface; a first dielectric layer (14) comprising molecules of a first compound, the molecules of the first compound having first ends and second ends, the first ends being covalently bonded to a first region of said substrate surface, said second ends having aromatic regions (paragraphs [0028], [0030] and [0035]); and a polycrystalline semiconductor layer (16) comprising organic semiconductor molecules with aromatic portions (paragraph [0036]), said polycrystalline semiconductor layer being on said first region of said substrate.

As to claim 2, Dimitrakopoulos et al., paragraph [0036] discloses that the organic semiconductor, embodied as pentacene, has molecules which comprise y conjugated pi-electrons, in which y is an integer of 10 or more, and said second ends of molecules of said first compound, embodied as a thiol (paragraph [0035]), comprise at least y minus 8 conjugated pi-electrons.

As to claim 5, Dimitrakopoulos et al., paragraph [0051], discloses that the molecules of the first compound may be bonded to said first region through a silicon bond.

As to claim 6, Dimitrakopoulos et al., paragraph [0036] discloses that the aromatic portions of said organic semiconductor molecules area adjacent to said aromatic regions of said first compound.

As to claim 7, Dimitrakopoulos et al., paragraph [0035] discloses that the first end and second end of the first dielectric layer may be interposed by a non-aromatic region comprising between 0 and about 16 carbon atoms, embodied as an organic structure R, shown in Figures 1(a) and 1(b), which may be a saturated or unsaturated cycloaliphatic structure.

As to claim 8, Dimitrakopoulos et al., Figure 4, discloses that a single crystal of said organic semiconductor molecules (16) is on about half of said first region.

As to claim 9, Dimitrakopoulos et al., Figure 4, discloses a gate electrode (12); a source electrode (20); and a drain electrode (20); said source and drain electrodes being in contact with a channel portion of said polycrystalline semiconductor layer on said first region, said gate electrode being positioned to control a conductivity of said channel portion.

As to claim 10, Dimitrakopoulos et al., Figure 4, discloses a second dielectric layer (18) comprising molecules of a second compound, the molecules of the second compound having third ends and fourth ends, said third ends being covalently bonded to a second region of said substrate surface, said fourth ends comprising no more than y minus 8 conjugated pi-electrons (paragraphs [0055] and [0056]).

As to claim 11, Dimitrakopoulos et al., Figure 5(h), discloses that the molecules of the first compound comprise three conjugated aromatic rings (paragraph [0058]).

As to claim 12, Dimitrakopoulos et al., Figure 4, discloses that the first and second regions form a pattern on the substrate (10).

Claims 13-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Dimitrakopoulos et al.. As to claim 13, Dimitrakopoulos et al., Figure 4, discloses a method of making a semiconductor apparatus, comprising the steps of: providing a substrate (10) having a substrate surface; providing a first dielectric layer (14) comprising molecules of a first compound, the molecules of the first compound having first ends and second ends, the first ends being covalently bonded to a first region of said substrate surface, said second ends having aromatic regions (paragraphs [0028], [0030] and [0035]); and providing a polycrystalline semiconductor layer (16) comprising organic semiconductor molecules with aromatic

portions (paragraph [0036]), said polycrystalline semiconductor layer being on said first region of said substrate.

As to claim 14, Dimitrakopoulos et al., paragraph [0036] discloses that method further provides that the organic semiconductor, embodied as pentacene, has molecules which comprise y conjugated pi-electrons, in which y is an integer of 10 or more, and said second ends of molecules of said first compound, embodied as a thiol (paragraph [0035]), comprise at least y minus 8 conjugated pi-electrons.

As to claim 15, Dimitrakopoulos et al., Figure 4, discloses providing a gate electrode (12); providing a source electrode (20); and providing a drain electrode (20); said source and drain electrodes being in contact with a channel portion of said polycrystalline semiconductor layer on said first region, said gate electrode being positioned to control a conductivity of said channel portion.

As to claim 16, Dimitrakopoulos et al., Figure 4, discloses that the solution of the organic semiconductor is applied to the first region (paragraph [0031]).

As to claim 17, Dimitrakopoulos et al., Figure 4, discloses providing a second dielectric layer (18) comprising molecules of a second compound, the molecules of the second compound having third ends and fourth ends, said third ends being covalently bonded to a second region of said substrate surface, said fourth ends comprising no more than y minus 8 conjugated pi-electrons (paragraphs [0055] and [0056]).

As to claim 18, Dimitrakopoulos et al., paragraphs [0017] and [0019], discloses patterning said first and second regions on said substrate.

Claim 19 is rejected under 35 U.S.C. 102(e) as being anticipated by Dimitrakopoulos et al.. Dimitrakopoulos et al., Figure 4, discloses an integrated circuit, comprising: a substrate (10) having a substrate surface; a first dielectric layer (14) comprising molecules of a first compound, the molecules of the first compound having first ends and second ends, the first ends being covalently bonded to a first region of said substrate surface, said second ends having aromatic regions (paragraphs [0028], [0030] and [0035]), a polycrystalline semiconductor layer (16) comprising organic semiconductor molecules with aromatic portions (paragraph [0036]), said polycrystalline semiconductor layer being on said first region of said substrate; a gate electrode (12); a source electrode (20); and a drain electrode (20); said source and

drain electrodes being in contact with a channel portion of said polycrystalline semiconductor layer on said first region, said gate electrode being positioned to control a conductivity of said channel portion.

Claim 20 is rejected under 35 U.S.C. 102(e) as being anticipated by Dimitrakopoulos et al.. Dimitrakopoulos et al., Figure 4, discloses a method of making an integrated circuit, comprising the steps of: providing a substrate (10) having a substrate surface; providing a first dielectric layer (14) comprising molecules of a first compound, the molecules of the first compound having first ends and second ends, the first ends being covalently bonded to a first region of said substrate surface, said second ends having aromatic regions (paragraphs [0028], [0030] and [0035]), providing a polycrystalline semiconductor layer (16) comprising organic semiconductor molecules with aromatic portions (paragraph [0036]), said polycrystalline semiconductor layer being on said first region of said substrate; providing a gate electrode (12); providing a source electrode (20); providing a drain electrode (20); and placing said source and drain electrodes in contact with a channel portion of said polycrystalline semiconductor layer on said first region, said gate electrode being positioned to control a conductivity of said channel portion.

Allowable Subject Matter

Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention with an organic semiconductor with a non-aromatic substituent.

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed invention where the molecules of the first compound are bonded to said first region through a sulfur bond.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

srw
January 19, 2005